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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,021	06/25/2001	Terry R. Lee	M4065.0407/P407	6645

24998 7590 06/16/2005

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,021	LEE, TERRY R.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,22-33 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,22-33 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20, 22-33 and 35 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-20, 22-33 and 35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter "shield line(s)" which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification discloses "shield" and "ground shield" which is the coupling between a pin of a connector to ground but not "shield line(s)" as claimed, e.g. *the pins 62 of connector 52 would be alternating between a signal line and ground, i.e., signal B0, ground, signal B1, ground, signal B2, ground, etc.*" (paragraph [0008]) and "*a ground shield 60 is provided on each side of the pair B2 and B3"* (paragraph [0023]). *The shields 60 provide a coupling path from the signal lines to ground"*. Applicant further claimed "*the shield lines* ***removably coupled***". The examiner found no support in the specification for this limitation either.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 26 recites the limitation "said first portion of said plurality of pins" in line 21. There is insufficient antecedent basis for this limitation in the claim.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "***a connector device... electrically connected to said processing unit and a circuit card coupled to said processing unit through said connector device***" (e.g. claim 19) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 5-9, 11-12, 14-16, 18-21, 24, 26-27, 29-31, and 33-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Robertson et al. (6,658,530) (hereinafter Robertson).

As to claim 1, Robertson teaches a circuit card (memory module 100) comprising: a circuit element supported by the circuit card, the circuit element having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B); a plurality of signal lines supported by the circuit card, each signal line being coupled respectively to one of said plurality of inputs or one of said plurality of outputs (Fig. 1A and col. 3, lines 47-67); and a plurality of shield lines supported by the circuit card (connection from ground pin 106 to ground) (at least col. 3 lines 60-62); wherein said signal lines are grouped in a plurality of adjacent corresponding pairs, a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines (Fig. 2B and col. 4, lines 57-67).

As to claim 2, Robertson further teaches each said shield line is a ground shield (ground) (col. 3, lines 62-67).

As to claim 5, Robertson further teaches the circuit element is a memory device (col. 4, lines 5-21).

As to claims 6, 8, 11, 15, 18, Robertson teaches a circuit card comprising: a plurality of signal lines (103) supported by the circuit card, each signal line being arranged and configured to be electrically and removably coupled at a first end respectively to one of a plurality of connectors of a connector device mounted on a printed circuit board (Fig. 1A and col. 3, lines 47-67); a circuit element (e.g. 107) mounted to the circuit card and having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B), said signal lines being coupled at a second end respectively to one of said plurality of inputs or outputs (Fig. 1A and col. 3, lines 47-67); and a plurality of shield lines (connection from ground pin 106 to ground) supported by the circuit card, the shield lines being arranged and configured to be electrically and removably coupled at a first end to respective connectors of said connector device mounted on said printed circuit board, each shield line being electrically coupled at a second end to a respective one of said plurality of circuit element inputs or outputs (Fig. 2B and col. 4, lines 57-67); said signal lines being grouped in a plurality of adjacent corresponding pairs, a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines; wherein said signal lines are part of a bus system (ground shields are arranged between a pair of signal lines) (Fig. 2B and col. 4, lines 57-67).

As to claims 7, 9, 12, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 14, Robertson further teaches the connector is adapted for connection to a motherboard (col. 3, lines 47-66 and col. 4, lines 40-59).

As to claim 16, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claims 19, 26, 30, 33, Robertson teaches a processing system comprising: a processing unit (e.g. CPU 1001); a connector device (102) having a plurality of connectors electrically connected to said processing unit and a circuit card (memory module 100) coupled to said processing unit through said connector device (col. 5 lines 40-59 and Figs. 4, 5), said circuit card comprising: a circuit element supported by the circuit card and having a plurality of inputs and outputs (Figs. 1A, 1B); a plurality of signal lines supported by the circuit card (connection from ground pin 106 to ground), each of said plurality of signal lines being removably coupled respectively between one of said plurality of inputs and one of said plurality of connectors, or one of said plurality of outputs and one of said plurality of connector (ground shields are arranged between a pair of signal lines) (Fig. 2B and col. 4, lines 57-67); said plurality of shield lines supported by the circuit card, each shield line being coupled respectively to said circuit element, said signal lines being grouped in a plurality of adjacent corresponding pairs, a shield line being located between respective corresponding pairs of said signal lines (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67, wherein said processing system comprises a bus system for passing signals

through said processing system and said signal lines are coupled to said bus system (Figs. 4-5 and col. 5 line 40 to col. 6 line 3As to claim 20, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 20, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 24, Robertson further teaches said circuit element is a memory device (col. 4, lines 5-21).

As to claim 27, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 29, Robertson further teaches a motherboard, equipped with a connector adapted for connection of said memory expansion card to said motherboard (col. 3, lines 47-66 and col. 4, lines 40-59).

As to claim 31, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Chin et al. (6,216,205) (hereinafter Chin).

As to claim 3, the argument above for claim 1 applies. However, Robertson does not explicitly disclose a driver to drive the signals between said inputs and said outputs of said circuit element. Chin teaches driver (I/O driver 16) to drive signals between inputs and outputs of an integrated circuit memory device (col. 8, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver as taught by Chin in the integrated circuit memory device of Robertson to for transferring data to and from the memory device (col. 8, lines 32-39).

As to claim 22, the argument above for claim 19 applies. However, Robertson does not explicitly disclose a driver to drive the signals between said inputs and said outputs of said circuit element. Chin teaches driver (I/O driver 16) to drive signals between inputs and outputs of an integrated circuit memory device (col. 8, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver as taught by Chin in the integrated circuit memory device of Robertson to for transferring data to and from the memory device (col. 8, lines 32-39).

6. Claims 4, 10, 13, 17, 23, 28, 32, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Ortega et al. (6,527,587) (herein after Ortega).

As to claim 4, the argument above for claim 1 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 10, the argument above for claim 8 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 13, the argument above for claim 11 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 17, the argument above for claim 15 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 23, the argument above for claim 19 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 28, the argument above for claim 26 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 32, the argument above for claim 30 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 35, the argument above for claim 33 applies. However, Robertson does not explicitly disclose adapting said first plurality of connectors in each

corresponding pair to conduct differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

7. Claims 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Elabd (6,526,462).

As to claim 25, the argument above for claim 19 applies. However, Robertson does not explicitly disclose the processing unit and the circuit element are on a same chip. Elabd teaches implementing the processor, memory, control unit, etc... on the same chip (col. 1, lines 22-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the processor and the integrated circuit on the same chip as taught by Elabd in the system of Robertson to provide a product that is smaller and faster (col. 1, lines 26-31).

Response to Arguments

8. Applicant's arguments filed 04-04-05 have been fully considered but they are not persuasive:

Regarding Applicant's arguments of "shield lines", first it is noted that "shield lines" are not disclosed in the specification as addressed in the 35 USC § 112 rejection above. Second, the Examiner found no distinguishing between "shield lines" of Applicant and "ground connection" of Robertson et al. since both discloses they are the connection between a pin of a connector to

ground (at least col. 3 lines 60-62) and provide shielding function to reduce interference or "crosstalk" (col. 3 line 63 to col. 3 line 4).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha Vu
Examiner
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